SDCONF-MAXV Datasheet

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1. General Description

SDCONF-MAXV provides a flexible FPGA configuration solution by the SD card for applications requiring compact size, high-speed operation and easy-to-use.

SDCONF-MAXV module performs configuration by using a common SD card to directly transfer binary data to FPGA devices. The SD card with up to 2GB formatted in FAT16 can be used for storing binary data. By a simple drag and drop operation in windows, binary data can be easily saved into the SD card and ready to use for configuration. There is no need of using JTAG cables.

With the use of a text file named CONFIG.TXT as a control file in the SD card, variety of parameters for configuration control such as binary data selection, delay setting, configuration mode changing, etc. can be specified by using a simple text editor, for example Notepad in windows. Any other specific software is not required.

A rotation 4-bit switch is provided to allow selecting up to 16 desired groups of binary files stored in a SD card for configuration. Each group of binary files is specified by a unique hexadecimal character in the control file CONFIG.TXT which corresponds to a value of switch. This solution brings the benefit of reduced debugging time in a development phase, because various binary data versions can be performed for comparison by using only one SD card. It also brings the benefit of convenience and flexibility in demonstration, since several different applications can be demonstrated without requiring to replace a new SD card.

SDCONF-MAXV module can interface with SD card at its maximum speed in fast mode which is up to 50MHz, and transfer binary data to FPGAs through a wide-changeable bus. Depending on configuration mode, the bus width can be set as 1-bit, 2-bit, 4-bit or 8-bit. SDCONF-MAXV provides most of the important configuration modes such as PS, PS with 2 or 4 parallel data lines, FPP, FPP with security and/or decompression. The speed of DCLK (CCLK) generated to FPGAs can be set by changing the speed parameter in the control file CONFIG.TXT. There are four levels of DCLK speed including 25 MHz (default), 12.5 MHz, 6.25 MHz and 3.125 MHz. Besides, the speed of DCLK is regulated automatically according to the configuration mode even though the speed parameter has no change. In FPP with security and/or decompress mode, each binary data byte is transferred to FPGAs by 4 cycles of DCLK. This function provides a reliable solution to protect customers' products effectively.

An arbitrary pre-amble is inserted to the head of binary data, and a post-amble with variable length followed immediately by the last byte of binary data is created to finish the configuration process. The value of pre-amble and post-amble can be specified in the control file CONFIG.TXT. In addition, the width of low level logic of nCONFIG signal and the interval from the instant nSTATUS signal goes high to the first generated DCLK can also be specified in the control file CONFIG.TXT.

2. Features and Benefits

- Configuration without JTAG cable
- Very short time of updating configuration data
- Simple configuration control with a text file
- Maximum operating frequency of 100 MHz
- Data transfer of 100 Mbps
- Security and/or decompress configuration
- Single and multiple FPGAs configuration
- Convenience and small-sized
- No requirement of an integrated software
- Selection of up to 16 groups of configuration data

3. Applications

SDCONF-MAXV is used for embedded system development, design verification, FPGA training and can also be used for various other domains.

4. Block Diagram

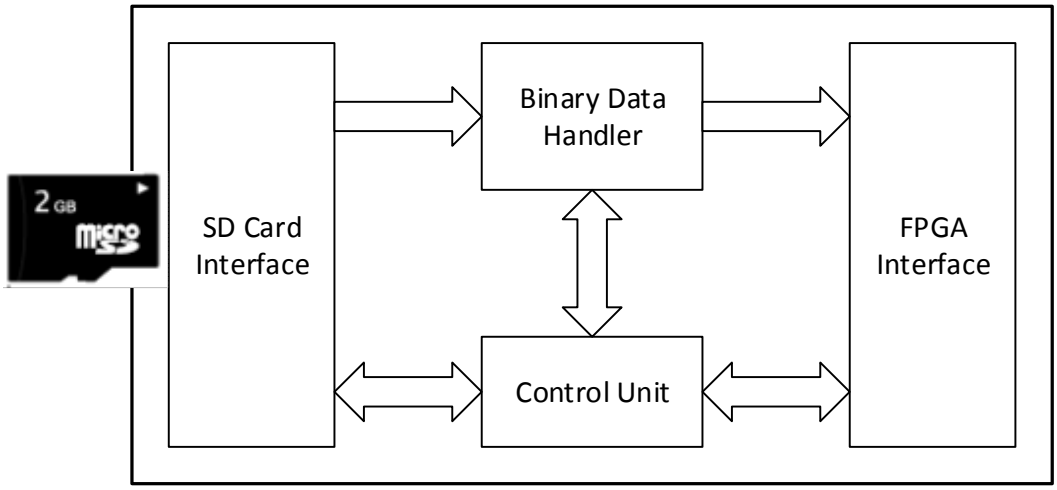


Figure 4.1. SDCONF-MAXV Block Diagram

5. Pin Descriptions and Switch Assignments

5.1. Pin Descriptions

SDCONF-MAXV has 32 pins of 1.27 mm haft pitch type arranged in horizontal lines.

Table 5.1. SDCONF-MAXV Pin Information

Pin No.	Signal Name	Dir	Inner Pull-up	Description
1	VCC3V3	–		3.3 V Power Input
2	VCCIO	–		VCCIO Power Input of IO signals
3	XAREA0	I	4.7K	Rotary switch 0 for selecting binary data (LSB)
4	XAREA1	I	4.7K	Rotary switch 1 for selecting binary data
5	XAREA2	I	4.7K	Rotary switch 2 for selecting binary data
6	XAREA3	I	4.7K	Rotary switch 3 for selecting binary data (MSB)
7	GND	–		GND
8	DONE	I	330Ω	FPGA DONE signal
9	DCLK	O		FPGA DCLK signal
10	nCONFIG	O	4.7K	FPGA nCONFIG signal
11	nSTATUS	I	4.7K	FPGA nSTATUS signal
12	XMODE0	I	4.7K	FPP/PS Mode selection
13	XCS0	O		Chip select signal for FPGA 0 control
14	XCS1	O		Chip select signal for FPGA 1 control

15	XCS4	O		Chip select signal for FPGA 4 control
16	XCS5	O		Chip select signal for FPGA 5 control
17	XCS6	O		Chip select signal for FPGA 6 control
18	XCS7	O		Chip select signal for FPGA 7 control
19	XCS2	O		Chip select signal for FPGA 2 control
20	XCS3	O		Chip select signal for FPGA 3 control
21	XMODE1	–	4.7K	NC
22	D0 / SOUT0	O		FPGA 8-bit parallel data 0 / serial data 0
23	D1	O		FPGA 8-bit parallel data 1
24	D2 / SOUT1	O		FPGA 8-bit parallel data 2 / serial data 1
25	D3	O		FPGA 8bit parallel data 3
26	GND	–		GND
27	D4 / SOUT2	O		FPGA 8-bit Parallel data 4 / serial data 2
28	D5	O		FPGA 8-bit parallel data 5
29	D6 / SOUT3	O		FPGA 8-bit parallel data 6 / serial data 3
30	D7	O		FPGA 8-bit parallel data 7
31	XMODE2	–	4.7K	NC
32	XRST	I	4.7K	Power-on-reset signal

Note:

a) XAREA[3:0], XMODE[2:0], DONE, nCONFIG are internal pull-up. External pull-ups are not required.
b) Externally terminal resistances are required for XCS[7:0].

5.2. Switch assignment

In control file CONFIG.TXT, 16 groups of binary data stored in the SD card can be assigned to the hexadecimal characters of from 0 to F, which are associated with 16 values of XAREA switch. Since XAREA[3:0] are negative logic signals, their reversed values are used to compare to the hexadecimal characters in control file CONFIG.TXT to determine which group of binary data is chosen for configuration. The XAREA logic levels and area assignments are expressed in Table 5.2. XAREA logic levels and area assignments
A part from using rotate switch, it is possible to control area assignments from a CPU.

Table 5.2. XAREA logic levels and area assignments

XAREA	Description

3	2	1	0	
H	H	H	H	Area 0
H	H	H	L	Area 1
H	H	L	H	Area 2
H	H	L	L	Area 3
H	L	H	H	Area 4
H	L	H	L	Area 5
H	L	L	H	Area 6
H	L	L	L	Area 7
L	H	H	H	Area 8
L	H	H	L	Area 9
L	H	L	H	Area A
L	H	L	L	Area B
L	L	H	H	Area C
L	L	H	L	Area D
L	L	L	H	Area E
L	L	L	L	Area F

6. Functional Description

6.1. Configuration Solutions

6.1.1. Configuration Voltage

SDCONF-MAXV module supports VCCIO voltage levels of 3.3 V ~ 2.5 V, and 1.8 V (rewriting of data is required).

The power supply of 3.0 V can be applied for 3.0 V VCCIO of Stratix-V.

In addition, voltage levels of 1.5 V and 1.2 V can also be applied only by rewriting data (but with special order).

6.1.2. Power-On-Reset Delay

Since there are a number of power supply voltages applied for FPGA, there might be a difference of the instant power supplies activate and those supply voltages reach their operating voltage levels.

If one of the supply voltages does not reach its operating level within tRAMP (200 µs ~ 100 ms), it is required to set up a Power-On-Reset (POR) delay. During the time of POR delay, FPGA must maintain nCONFIG at low level logic.

SDCONF-MAXV module releases nCONFIG after about 1.96 msec(s) from the time when XRST is released. On the FPGA side, nCONFIG must also be released when the low level logic of this signal is detected. The configuration is started after nCONFIG goes high level logic due to a pull-up resistance.

It is required to turn off the pump on function by pre-setting parameter C1 to “0” (default) in control file CONFIG.TXT (refer Command Definitions for more detail).

Figure 8–2. Relationship between t_{RAMP} and POR Delay

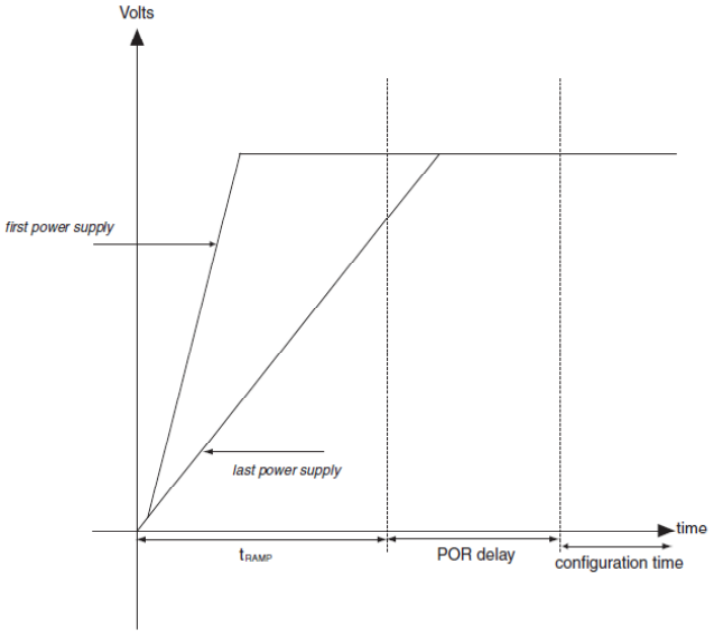


Figure 6.1. Relationship between tRAMP and POR delay

Table 9–2. Fast and Standard POR Delay Specification ***(Note 1)***

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Figure 6.2. Fast and Standard POR Delay Specification

6.2. Configuration Modes

6.2.1. FPP

SDCONF-MAXV module supports FPP configuration mode with bus width of 8-bit. In this mode, the XMODE0 pin must be set to the low level logic.

6.2.2. PS

SDCONF-MAXV module supports PS configuration mode, and it is selected by setting the XMODE0 pin to the high level logic.

6.2.3. AS

SDCONF-MAXV module does not support AS configuration mode. However, it is considering to be provided in the future. Please contact for more detail.

6.2.4. Security

SDCONF-MAXV module can handle encrypted binary data as usual without any intervention. Normally, when encrypted binary data transferred to FPGA are decrypted by the right key, the configuration is completed. Otherwise, the configuration is not terminated.

In FPP mode, if AES is used, parameter C5 is required to be set to “1” in order to output 4 cycles of DCLK for each binary byte. This is not required for PS mode.

6.2.5. Decompression

SDCONF-MAXV module can handle binary data with security and/or decompression.

In FPP mode, if decompression is used, parameter C5 is required to be set to “1” in order to output 4 cycles of DCLK for each binary byte. This is not required for PS mode.

6.3. Single-FPGA Configuration

- FPP/PS Mode Combination

Figure of FPP/PS combination

- Fixed PS Mode

Figure of fixed PS connection

6.4. Multi-FPGA Configuration

Figure of multiple FPGAs connection

7. LED Description

SDCONF-MAXV module provides a green LED for expressing working statuses.

Table 7.1. LED Meanings

LED status	Meaning
Lighting	Transferring binary data from SD card
Light out	Transmission of binary data from SD card is completed
Not lighting	SD card is not inserted

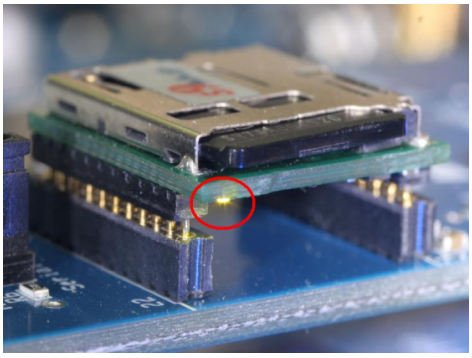


Figure 7.1. Status LED

8. Command Definitions

Introduction of “CONFIG.TXT” file

8.1. CONFIG.TXT Construction

Sample of CONFIG.TXT

8.2. Command Set

8.2.1. “/”

8.2.2. “S : 0/1/2/3”

8.2.3. “P : SS”

8.2.4. “P : SB”

8.2.5. “P : PR”

8.2.6. “P : PM”

8.2.7. “P : PO”

8.2.8. “P : D1”

8.2.9. “P : D2”

8.2.10. “P : C1/2/3/4/5”

8.2.11. “# 0 ÷ F : <Bit File Name>”

* Bit file separation:

8.3. D1, D2, PO Settings

Table of Reference Values of D1, D2, PO

8.4. Default Parameter Values

Table of Default Parameter Values

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

10. Timing Diagrams

10.1. Block Diagram of Output Signals

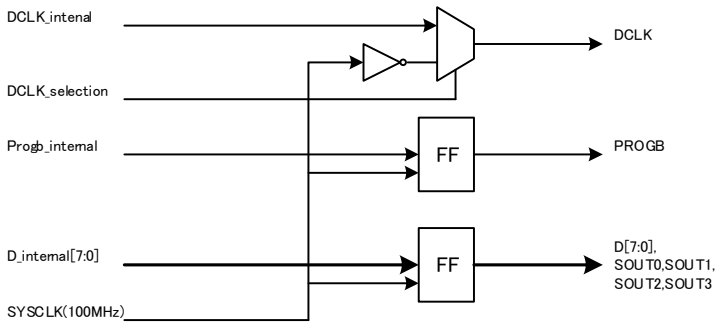


Figure 10.1. Block Diagram of Output Signals

10.2. Timing Diagram

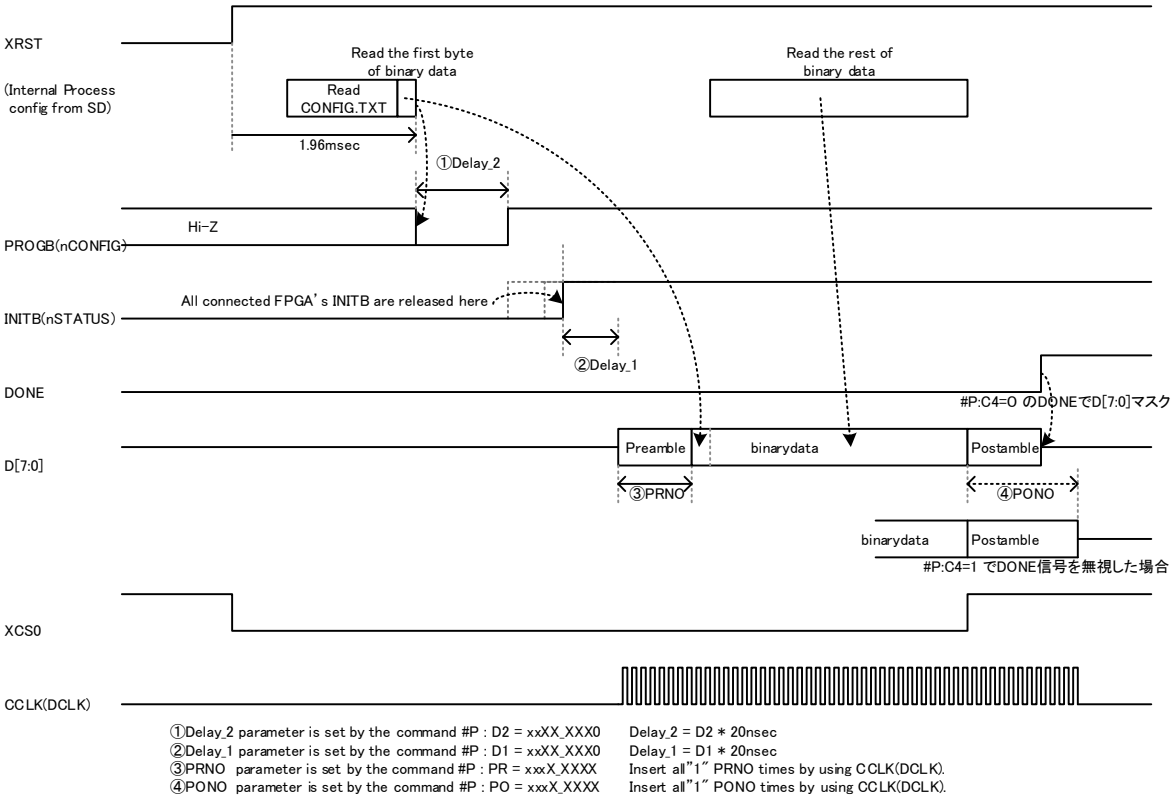


Figure 10.2. Time Chart for Single FPGA Connection

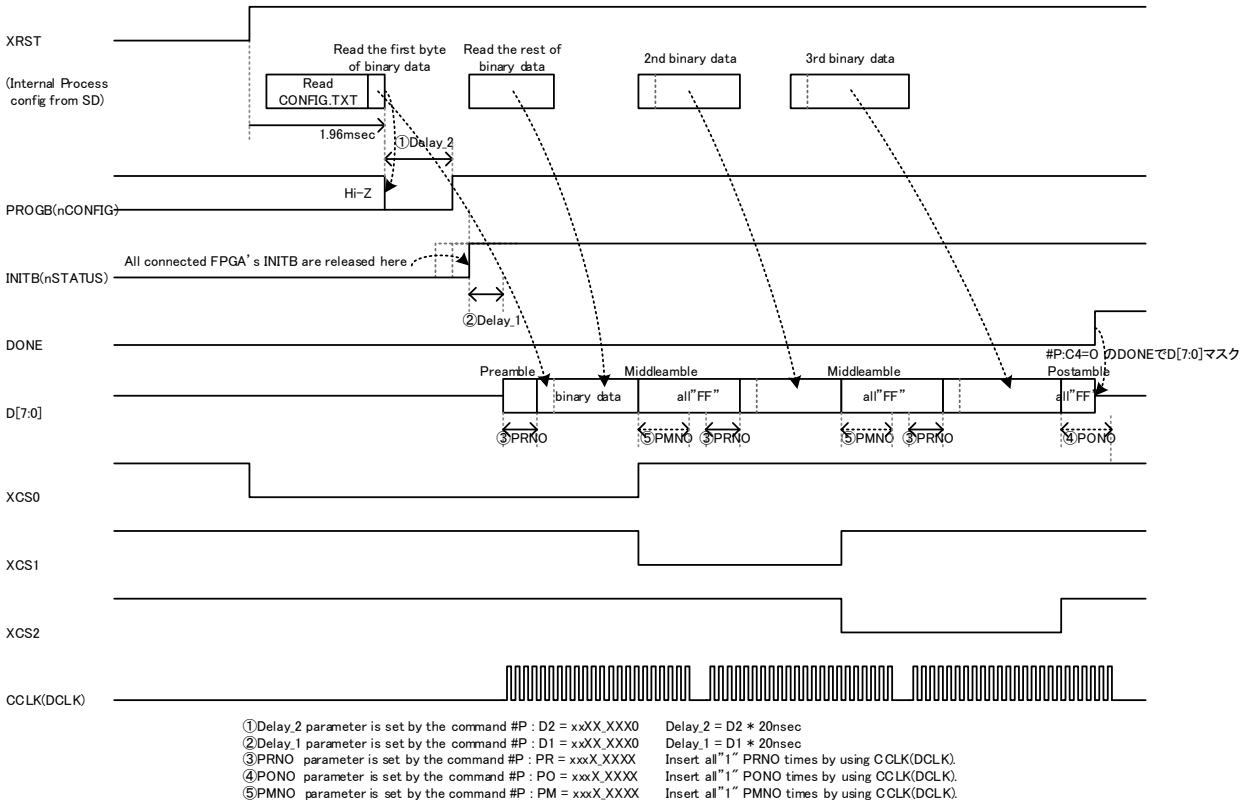


Figure 10.3. Time Chart for Multiple FPGAs Connection

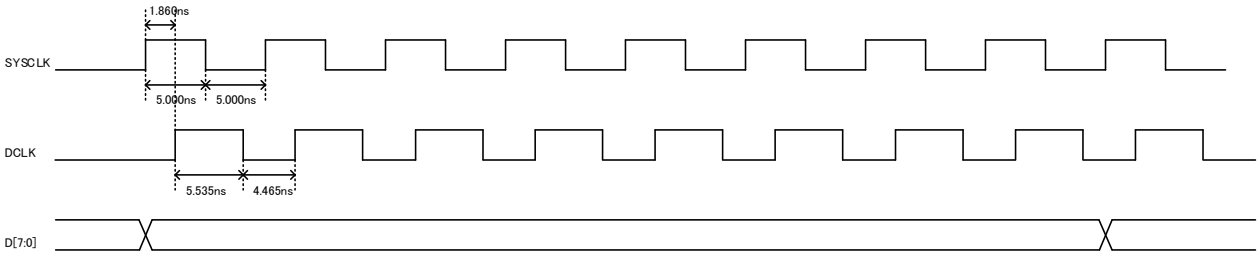


Figure 10.4. Wave Form of DCLK (CCLK) at 100 MHz

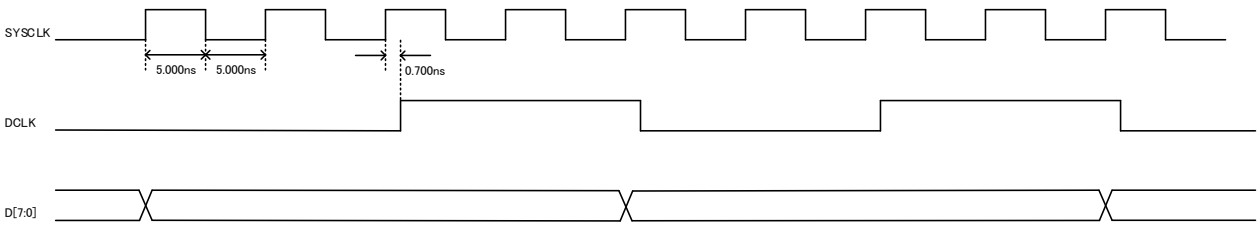
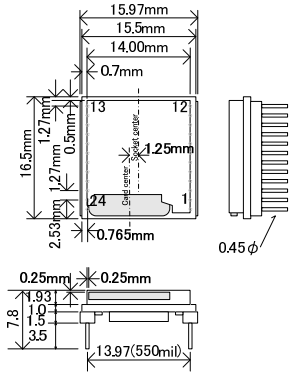


Figure 10.5. Wave Form of DCLK (CCLK) at 25 MHz

11. Package Dimensions



12. Product Update